

	Type	L #	Hits	DBs	Search Text	Time Stamp
16	BRS	L22	18	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	L21 and logic and (vector same space)	2007/06/11 14:49
17	BRS	L23	0	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(westphall-jonathan).in.	2007/06/11 14:51
18	BRS	L24	8	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(westphal-jonathan).in.	2007/06/11 14:51

	Type	L #	Hits	DBs	Search Text	Time Stamp
1	BRS	L7	1	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	"5379231".pn. and logic	2007/06/11 14:36
2	BRS	L8	759	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(computer same program) and (logic same circuit same reduction)	2007/06/11 14:37
3	BRS	L9	193	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(computer same program) and (logic same circuit same reduction) and (gate same reduction)	2007/06/11 14:37
4	BRS	L10	10	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(computer same program) and (logic same circuit same reduction) and (gate same reduction) and (vector same space)	2007/06/11 14:40
5	BRS	L11	0	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(gate same reduction).ti.	2007/06/11 14:38

	Type	L #	Hits	DBs	Search Text	Time Stamp
6	BRS	L13	2	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(vector adj space) same (logic same circuit) and rules	2007/06/11 14:41
7	BRS	L12	8	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(vector adj space) same (logic same circuit)	2007/06/11 14:41
8	BRS	L14	3	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(gate adj reduction) same rules	2007/06/11 14:44
9	BRS	L15	17	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(state adj tables) same reduction	2007/06/11 14:45
10	BRS	L16	0	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(state adj tables) same reduction and (vector adj space)	2007/06/11 14:45

	Type	L #	Hits	DBs	Search Text	Time Stamp
11	BRS	L18	242	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	703/1.ccls. and pd>= "20061127" and logic	2007/06/11 14:46
12	BRS	L17	953	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	703/1.ccls. and pd>= "20061127"	2007/06/11 14:46
13	BRS	L19	14	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	703/1.ccls. and pd>= "20061127" and logic and (vector same space)	2007/06/11 14:47
14	BRS	L20	18	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	716/1.ccls. and pd>= "20061127" and logic and (vector same space)	2007/06/11 14:47
15	BRS	L21	1702	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	716/1.ccls. and pd>= "20061127"	2007/06/11 14:48


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)

Scholar All articles - Recent articles Results 1 - 10 of about 135 for "A Gate-Level Leakage Power Reduction"

[All Results](#)
[M Johnson](#)
[K Roy](#)
[D Blaauw](#)
[F Najm](#)
[J Halter](#)

A gate-level leakage power reduction method for ultra-low-power CMOS circuits - all 7 versions »

JP Halter, FN Najm - Custom Integrated Circuits Conference, 1997., Proceedings of ..., 1997 - ieeexplore.ieee.org

Page 1. **A Gate-Level Leakage Power Reduction** Method for Ultra-Low-Power CMOS Circuits Jonathan P. Halter and Farid N. Najm ECE Dept. ...

Cited by 133 - Related Articles - Web Search - BL Direct

Estimation of standby leakage power in CMOS circuits considering accurate modeling of transistor ... - all 8 versions »

Z Chen, M Johnson, L Wei, K Roy - Proceedings of the 1998 international symposium on Low power ..., 1998 - portal.acm.org

Page 1. Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks Zhanping Chen, Mark ...

Cited by 145 - Related Articles - Web Search

Scaling of stack effect and its application for leakage reduction - all 6 versions »

»

S Narendra, V De, D Antoniadis, A Chandrakasan, S ... - Proceedings of the 2001 international symposium on Low power ..., 2001 - portal.acm.org

... [8] JP Halter and F. Najm, "A gate-level leakage power reduction method for ultra-low-power CMOS circuits," Custom Integrated Circuits Conf., pp. ...

Cited by 82 - Related Articles - Web Search

Evaluating run-time techniques for leakage power reduction - all 14 versions »

D Duarte, YF Tsai, N Vijaykrishnan, MJ Irwin - Design Automation Conference, 2002.

Proceedings of ASP-DAC ..., 2002 - ieeexplore.ieee.org

Page 1. □ Acknowledgment: This research is supported in part by MARCO-GSRC grant 98-DT-660, NSF Career Award 0093085 and donations from Intel Corp. Abstract ...

Cited by 59 - Related Articles - Web Search

Leakage control with efficient use of transistor stacks in single threshold CMOS - all 14 versions »

MC Johnson, D Somasekhar, LY Chiou, K Roy - IEEE Transactions on Very Large Scale Integration(VLSI) ..., 2002 - doi.ieeecomputersociety.org

... 59-63. [4] Halter, JP, and Najm, F. **A gate-level leakage power reduction** method for ultra-low-power CMOS circuits. Proceedings of ...

Cited by 88 - Related Articles - Web Search - BL Direct

Design methodology for fine-grained leakage control in MTCMOS - all 7 versions »

BH Calhoun, FA Honore, A Chandrakasan - Proceedings of the 2003 international symposium on Low power ..., 2003 - portal.acm.org

... [5] JP Halter and F. N.Najm, "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits", CICC, 1997. [6 ...

Cited by 37 - Related Articles - Web Search

Duet: an accurate leakage estimation and optimization tool for dual-Vt circuits

- all 4 versions »

S Sirichotiyakul, T Edwards, C Oh, R Panda, D ... - IEEE Transactions on Very Large Scale Integration (VLSI) ..., 2002 - portal.acm.org

... 16, pp. 343-352, 1997. 14 J. Halter and FN Najm, "A gate-level leakage power reduction method for ultra-low-power CMOS circuits," in Proc. ...

Cited by 36 - Related Articles - Web Search - BL Direct

Robust SAT-Based Search Algorithm for Leakage Power Reduction - all 6

versions »

FA Aloul, S Hassoun, KA Sakallah, D Blaauw - Proceedings of the 12th International Workshop on Integrated ..., 2002 - Springer

... 1998. 7. J. Halter and F. Najm, "A gate-level leakage power reduction method for ultra-low-power CMOS circuits," in Proc. of ...

Cited by 24 - Related Articles - Web Search - BL Direct

Leakage power analysis and reduction during behavioral synthesis - all 7

versions »

KS Khouri, NK Jha - Very Large Scale Integration (VLSI) Systems, IEEE ..., 2002 - ieeexplore.ieee.org

Page 1. 876 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL.

10, NO. 6, DECEMBER 2002 Leakage Power Analysis and Reduction ...

Cited by 32 - Related Articles - Web Search - BL Direct

Runtime mechanisms for leakage current reduction in CMOS VLSI circuits -

all 6 versions »

AF Abdollahi, F Massoud - Low Power Electronics and Design, 2002. ISLPED'02. ..., 2002 - ieeexplore.ieee.org

Page 1 Runtime Mechanisms for Leakage Current Reduction in CMOS VLSI Circuits1'2 Afshin Abdollahi Farzan Fallah Massoud Pedram University of Southern ...

Cited by 26 - Related Articles - Web Search

Google ►

Result Page: 1 2 3 4 5 6 7 8 9 10 [Next](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2007 Google


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)

Scholar All articles - Recent articles Results 11 - 20 of about 715 for **gate reduction logic circuit "vector space"**

All Results

[P Shor](#)
[A Barenco](#)
[M Nielsen](#)
[D DiVincenzo](#)
[C Bennett](#)

Designing logic circuits for probabilistic computation in the presence of noise - all 4 versions »

K Nepal, RI Bahar, J Mundy, WR Patterson, A ... - Proceedings of the 42nd annual conference on Design ..., 2005 - portal.acm.org

... limits, with the ultimate transistor **gate** length near L ... a digital computation **circuit**, and the **reduction** of **logic** ... a **circuit** with hundreds of **logic** variables it ...

Cited by 10 - Related Articles - Web Search

Topological analysis for leakage prediction of digital circuits - all 7 versions »

W Jiang, V Tiwari, E de la Iglesia, A Sinha - Design Automation Conference, 2002.

Proceedings of ASP-DAC ..., 2002 - ieeexplore.ieee.org

... Analytical models for leakage **reduction** in stacks have been studied in ... leakage current for a fully static four-input **NAND gate**. ... inputs a,b,c,d are at **logic** zero ...

Cited by 20 - Related Articles - Web Search

On the over-specification problem in sequential ATPG algorithms - all 6 versions »

KT Cheng, HKT Ma - Computer-Aided Design of Integrated Circuits and Systems, ..., 1993 - ieeexplore.ieee.org

... YL Lin, "Channel density **reduction** by routing density **reduction** by routing ... is implemented in two-level AND-OR **logic** with each AND **gate** corresponding to ...

Cited by 20 - Related Articles - Web Search - BL Direct

[CITATION] Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer - all 55 versions »

PW Shor - SIAM Review, 1999 - Society for Industrial and Applied Mathematics

... model is analogous to classical acyclic **circuits** in theoretical ... 3. Reversible **Logic** and Modular Exponentiation ... The definition of quantum **gate** arrays gives rise ...

Cited by 1240 - Related Articles - Web Search - BL Direct

Simulating the Effect of Decoherence and Inaccuracies on a Quantum Computer - all 7 versions »

KM Obenland, AM Despain - Proc. 1st NASA Conference on Quantum Computation and Quantum ..., 1998 - Springer

... a **logic** zero with the ground state of an ion, and a **logic** one with a ... the shift in the peak values causes a further **reduction** in the ... 3.4 The Error Rate per **Gate** ...

Cited by 12 - Related Articles - Web Search - BL Direct

Macromodeling and Optimization of Digital MOS VLSI Circuits - all 8 versions »

»

MD Matson, LA Glasser - Computer-Aided Design of Integrated Circuits and Systems, ..., 1986 - ieeexplore.ieee.org

... approach inappropriate for high-performance **circuit** design. Other authors have aimed for fast computation times by simplifying both the **logic gate** models and ...

Cited by 39 - Related Articles - Web Search - Library Search

An efficient comparative concurrent Built-In Self-Test technique - all 3

[versions »](#)

I Voyatzis, D Nikolos, A Paschalidis, C Halatsis, T ... - Test Symposium, 1995., Proceedings of the Fourth Asian, 1995 - ieeexplore.ieee.org

... R, we can compromise between the hardware overhead needed and the **reduction** in test ...

gate, the n-input OR **gate**, the n-input NOR **gate**, the D ... Figure 4: Logic Cell ...

Cited by 6 - Related Articles - Web Search

A METHODOLOGY FOR THE COMPUTATION OF AN UPPER BOUND ON NOISE CURRENT SPECTRUM OF CMOS SWITCHING ... - all 7 versions »

A Nardi, H Zeng, JL Garrett, L Daniel, AL ... - Proceedings of the International Conference on Computer Aided ... - doi.ieeecomputersociety.org

... Even though the entire **logic** space is ex- plored by the algorithm ... If the same notation introduced above for a **gate** is now used for a **circuit** block with p ...

Cited by 8 - Related Articles - Web Search - Library Search - BL Direct

FASER: Fast Analysis of Soft Error Susceptibility for Cell-Based Designs - all 6 versions »

B Zhang, WS Wang, M Orshansky - Proceedings of the 7th International Symposium on Quality ..., 2006 - portal.acm.org

... yet efficiently accounting for the **reduction** of error ... SER de-ratings due to electrical, **logic**, and latching ... on the specific transistor network of each **gate** ...

Cited by 7 - Related Articles - Web Search

A Heuristic to Determine Low Leakage Sleep State Vectors for CMOS Combinational Circuits - all 7 versions »

RM Rao, F Liu, JL Burns, RB Brown - Proceedings of the International Conference on Computer Aided ... - doi.ieeecomputersociety.org

... a very effective approach for leakage **reduction** without significant ... cell C 0 should be at **logic** 0 state ... total leakage (ie, sub-threshold plus **gate** leakage) in ...

Cited by 9 - Related Articles - Web Search - BL Direct

◀ Gooooooooooooogle ▶

Result Page: [Previous](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [Next](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2007 Google

	Type	L #	Hits	DBs	Search Text	Time Stamp
1	BRS	L8	174	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(logic same (simplify simple) same circuits) and (vector same space)	2007/06/11 15:07
2	BRS	L9	103	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	(logic same (simplify simple) same circuits) and (vector same space) and ((simple simpler) same form)	2007/06/11 15:07